~~a.~~ a semiconductor substrate;

~~b.~~ a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

~~c.~~ a metallic wall comprising two spaced-apart sides in the layer of dielectric material; and

~~d.~~ a wall of insulation material only between the metallic wall and the periphery of the integrated circuit device, wherein the insulation material and dielectric material are different materials.

REMARKS

Claims 9 to 16 and 18 are pending in the present application. Claims 9, 11, 16 and 18 have been amended for which there is support in the specification, claims and drawings as originally filed.

Reconsideration of the Examiner's decisions and reexamination of this application are respectfully requested.

Examiner interview:

The Examiner's courtesy in granting an interview with the undersigned on April 22, 2005, is acknowledged. During the interview, the undersigned discussed with the Examiner amendments to claims 9, 16 and 18 and the references cited by the Examiner. Among the amendments discussed, the undersigned proposed amending claims 9, 16 and 18 so as to positively recite the edge seal attributes of the invention in the main body of the claim. The Examiner appeared to be favorably disposed to such a proposal.

The specification:

The specification has been amended so as to include the continuing data, that the present application is a divisional.

The §102 rejections:

The claims have been amended to clarify and distinguish the invention. Claims 9, 16 and 18 have been amended to positively recite an edge seal structure as part of the main body of the claims. Claim 9 has been further amended to make clear that the layer of insulating material

isolates the metallic wall from both the low-k dielectric material and an overlying or underlying hard material layer. Claim 16 has been further amended to recite that the two metallic walls are physically connected as clearly shown in Figures 3E, 3F and 4D. And, claim 18 has been further amended to make clear that the wall of insulation material is only on one side of the metallic wall, i.e., the side facing the periphery of the integrated circuit device.

I. Claims 9 to 16 and 18 have been rejected by the Examiner under 35 USC §102(b) as being anticipated by Wetzel U.S. Patent 6,143,646 (hereafter "Wetzel").

Claim 9 is distinuishable from Wetzel in that Wetzel relates to a semiconductor wiring structure whereas Applicants' invention relates to an edge seal structure. Any teaching from Wetzel relating to the desirable electrical attributes of the semiconductor wiring structure would seem to not be applicable to the mechanical requirements (i.e., stopping cracks) of Applicants' edge seal structure. Moreover, Claim 9 has been amended to include a "layer of hard material over or under" the low-k dielectric material and the layer of insulation material of the edge seal structure is interposed between the metallic wall and the low-k dielectric material as well as between the metallic wall and the hard material. Referring, for example, to Figure 10 of Wetzel, there is a layer of hard material, oxide 22, underlying the low-k dielectric material 30, which is in contact with metallic barrier 41 and/or metallic layer 40 which is the kind of structure avoided by the present invention. However, there is no layer in Wetzel equivalent to Applicants' layer of insulation. Accordingly, Wetzel cannot anticipate Applicants' claim 9.

Claim 16 is distinguishable from Wetzel in several respects. First, claim 16 relates to an edge seal structure whereas Wetzel relates to a semiconductor wiring structure as explained above. Second, claim 16 recites "two spaced-apart metallic walls physically connected by a metallic cross piece". Referring to Figure 10, for example, of Wetzel, it can be seen that there are metallic walls such as 38, 40 or 42. Each of the metallic walls are spaced-apart but not also physically connected, such as walls 40 and 42, or metallic walls that are physically connected but not also spaced-apart, such as walls 38 and 40. As Wetzel cannot meet the limitations of Applicants' claim 16, claim 16 cannot be anticipated by Wetzel.

Claim 18 is distinguishable from Wetzel in several respects. First, claim 18 relates to an edge seal structure whereas Wetzel relates to a semiconductor wiring structure as explained above. Second, claim 18 claims a wall of insulation material only on one side of the metallic wall. Again referring to Figure 10 of Wetzel, oxide material 22 is on both sides of metallic wall 30. As Wetzel cannot meet the limitations of claim 18, claim 18 cannot be anticipated by Wetzel.

Inasmuch as claims 10 to 15 depend from claim 9, and since claim 9 is believed to be allowable, then claims 10 to 15 should be allowable as well. No independent ground of patentability is asserted for claims 10 to 15 at this time.

II. Claims 9 to 16 and 18 have been rejected by the Examiner under 35 USC §102(b) as being

anticipated by Chooi et al. U.S. Patent 6,372,636 (hereafter "Chooi").

Claim 9 is distinuishable from Chooi in that Chooi relates to a semiconductor wiring structure whereas Applicants' invention relates to an edge seal structure. Any teaching from Chooi relating to the desirable electrical attributes of the semiconductor wiring structure would seem to not be applicable to the mechanical requirements (i.e., stopping cracks) of Applicants' edge seal structure. Moreover, Claim 9 has been amended to include a "layer of hard material over or under" the low-k dielectric material and the layer of insulation material of the edge seal structure is interposed between the metallic wall and the low-k dielectric material as well as between the metallic wall and the hard material. In Chooi, this layer of hard material would correspond to etch stop layer 225/325/425.Chooi does disclose a layer of insulation material which are silicon spacers 250/350/450 but this layer of insulation material is not complete in that etch stop layer 225/325/425 contacts the metallic wall (i.e., barrier 41 or the copper fill material). Applicants' claim 9, however, recites "a layer of insulation material between the metallic wall and the low-k dielectric material and between the metallic wall and the layer of hard material" Whereas Chooi discloses a structure wherein the metallic wall is in contact with the layer of hard material, Applicants require that the layer of insulation material be between the metallic wall and the layer of hard material. Thus, Chooi cannot meet the limitations of Applicants' claim 9. Accordingly, Chooi cannot anticipate Applicants' claim 9.

Claim 16 is distinguishable from Chooi in several respects. First, claim 16 relates to an edge seal structure whereas Chooi relates to a semiconductor wiring structure as explained above.

Second, claim 16 recites "two spaced-apart metallic walls physically connected by a metallic cross piece". Referring to Chooi, it can be seen that there are no two spaced-apart metallic walls which are also physically connected. Realistically, there will be multiple copper fill areas while only one is shown in Chooi. However, these multiple copper fill areas will also not be connected since Chooi relates to semiconductor wiring and connecting these copper fill areas will result in an unacceptable electrical short situation. Therefore, as Chooi cannot meet the limitations of Applicants' claim 16, claim 16 cannot be anticipated by Chooi.

Claim 18 is distinguishable from Chooi in several respects. First, claim 18 relates to an edge seal structure whereas Chooi relates to a semiconductor wiring structure as explained above. Second, claim 18 claims a wall of insulation material only on one side of the metallic wall. Again referring to the figures of Chooi, etch stop layer 225/325/425 and silicon spacers 250/350/450 are on both sides of the copper fill. As Chooi cannot meet the limitations of claim 18, claim 18 cannot be anticipated by Chooi.

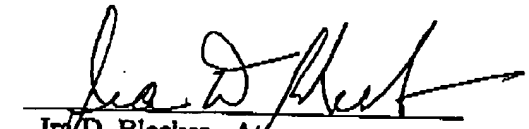
Inasmuch as claims 10 to 15 depend from claim 9, and since claim 9 is believed to be allowable, then claims 10 to 15 should be allowable as well. No independent ground of patentability is asserted for claims 10 to 15 at this time.

Summary:

In view of all of the preceding remarks, it is submitted that all of claims 9 to 16 and 18 are in condition for allowance. If the Examiner finds this application deficient in any respect, the Examiner is invited to telephone the undersigned at the Examiner's earliest convenience to resolve such deficiency.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
, et al.

By: 

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